QDD EDFA Datasheet

Features

- QSFP-DD Compact Form
- Hot Pluggable
- Duplex LC Connector
- Output Power Monitoring
- I2C Communication Interface

Version History

Date	Version	Description
2024/12/31	1.0	Initialize

Order Information

Taclink Part Number	Description	Code
WZEDFA-EM-BQD01606-LC/UPC	-	-

Functional Diagram

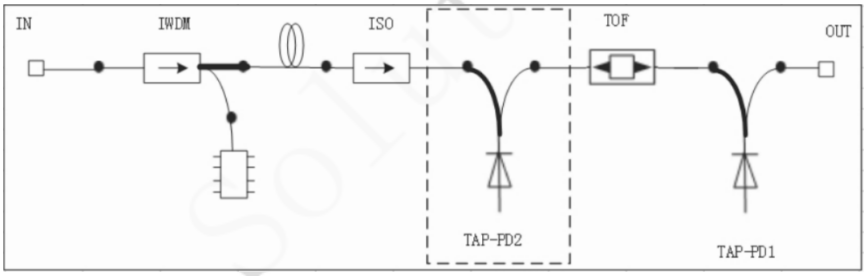


Figure1 Functional Diagram

Operation/Storage Temperature and Humidity

Parameter	Specification	Unit	Note
Operating case temperature	-5 ~ 75	℃	
Operation Humidity	5~90	%RH	
Storage Temperature	-25 ~ +85	℃	
Storage Humidity	5~95	%RH	

Optical Characteristics

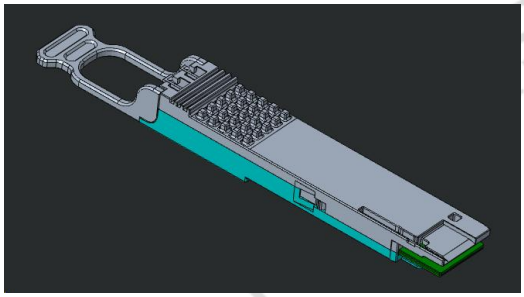
Parameter	Min	Typ	Max	Units	Comments
Wavelength range	1528		1565	nm	1ch.
Signal input power	-13		-10	dBm	
Signal input power monitoring range	-16		-6	dBm	
Output power	6			dBm	
Noise figure		6	7	dB	Test Condition : Pin = -13dBm, Pout=6dBm.
Output power monitor accuracy	-0.5		0.5	dB	

Polarization-mode dispersion			0.5	ps	
Polarization dependent gain			0.5	dB	
Return loss	30			dB	
TOF Characteristics					
3 dB Bandwidth	160	180	220	GHz	
20 dB Bandwidth	350	480	560	GHz	
Side-mode Suppression Ratio		30		dB	
Temperature dependence frequency shift	-55		55	GHz	

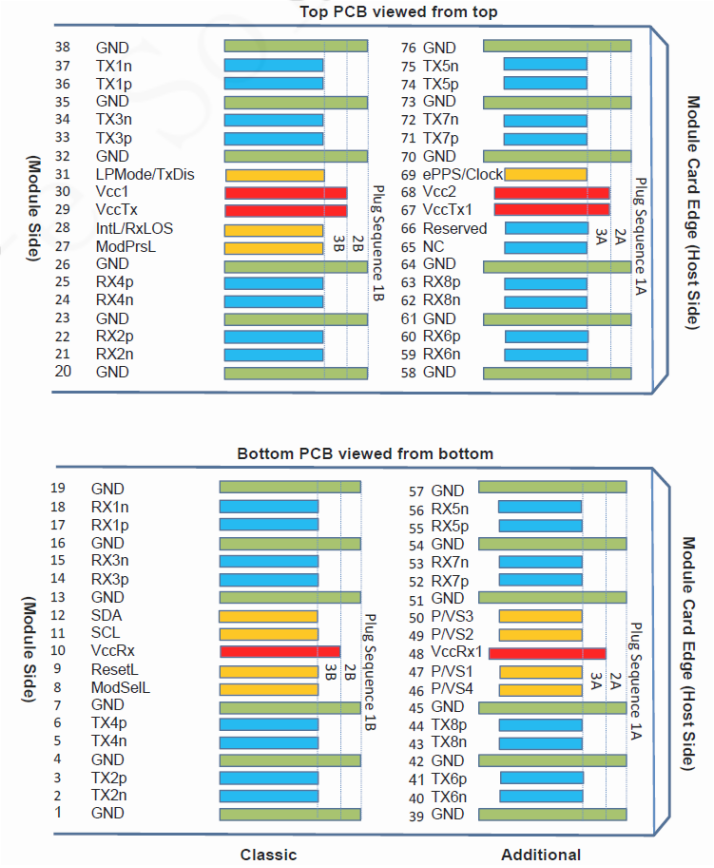
Mechanical Dimension Part

Compliant with QSFP-DD MSA .

Layout



Hardware Interface



Pad	Pin Name	Logic	Function	Plug Seq.	Notes
1	GND		Ground	1B	1
2	Tx2n	CML	Reserve	3B	6
3	Tx2p	CML	Reserve	3B	6
4	GND		Ground	1B	1
5	Tx4n (TXD)	LVTTL	Serial Port Output	3B	6
6	Tx4p (RXD)	LVTTL	Serial Port Input	3B	6
7	GND		Ground	1B	1
8	ModSelL	LVTTL	Module Select	3B	7
9	ResetL	LVTTL	Module Reset	3B	8
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVCMOS	TWI serial interface clock	3B	
12	SDA	LVCMOS	TWI serial interface data	3B	
13	GND		Ground	1B	1
14	Rx3n	CML	Reserve	3B	6
15	Rx3n	CML	Reserve	3B	6
16	GND		Ground	1B	1
17	Rx1n	CML	Reserve	3B	6
18	Rx1n	CML	Reserve	3B	6
19	GND		Ground	1B	1
20	GND		Ground	1B	1
21	Rx2n	CML	Reserve	3B	6
22	Rx2n	CML	Reserve	3B	6
23	GND		Ground	1B	1
24	Rx4n	CML	Reserve	3B	6
25	Rx4n	CML	Reserve	3B	6
26	GND		Ground	1B	1
27	ModPrsL	LVTTL	Module Present	3B	10
28	IntL	LVTTL	Interrupt	3B	11
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	TxDis	LVTTL	Optional TX Disable	3B	9
32	GND		Ground	1B	1
33	Tx3n	CML	Reserve	3B	6
34	Tx3p	CML	Reserve	3B	6
35	GND		Ground	1B	1
36	Tx1n	CML	Reserve	3B	
37	Tx1p	CML	Reserve	3B	
38	GND		Ground	1B	1
39	GND		Ground	1A	1
40	Tx6n	CML	Reserve	3A	6
41	Tx6p	CML	Reserve	3A	6
42	GND		Ground	1A	1
43	Tx8n	CML	Reserve	3A	6
44	Tx8p	CML	Reserve	3A	6
45	GND		Ground	1A	1

46	P/VS4	LVCMOS/CML	Programmable/Module Vendor Specific 4	3A	5
47	P/VS1	LVCMOS/CML	Programmable/Module Vendor Specific 1	3A	5
48	VccRx1		3.3V Power Supply	2A	2
49	P/VS2	LVCMOS/CML	Programmable/Module Vendor Specific 2	3A	5
50	P/VS3	LVCMOS/CML	Programmable/Module Vendor Specific 3	3A	5
51	GND		Ground	1A	1
52	Rx7n	CML	Reserve	3A	6
53	Rx7n	CML	Reserve	3A	6
54	GND		Ground	1A	1
55	Rx5n	CML	Reserve	3A	6
56	Rx5n	CML	Reserve	3A	6
57	GND		Ground	1A	1
58	GND		Ground	1A	1
59	Rx6n	CML	Reserve	3A	6
60	Rx6n	CML	Reserve	3A	6
61	GND		Ground	1A	1
62	Rx8n	CML	Reserve	3A	6
63	Rx8n	CML	Reserve	3A	6
64	GND		Ground	1A	1
65	NC		No Connect	3A	3
66	Reserve		For future use	3A	3
67	VccTx1		3.3V Power Supply	2A	3
68	Vcc2		3.3V Power Supply	2A	3
69	ePPS/Clock	LVCOM	Reserve	3A	6
70	GND		Ground	1A	1
71	Tx7n		Reserve	3A	6
72	Tx7p		Reserve	3A	6
73	GND		Ground	1A	1
74	Tx5n		Reserve	3A	6
75	Tx5p		Reserve	3A	6
76	GND		Ground	1A	1

Note1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500 mA.

Note2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be connected together. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table3.1. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 2000 mA.

Note3: Reserved pad recommended to be terminated with 10kΩto ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10kΩ to ground on the host.

Note4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (See Figure6.1 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note5: Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10k.

Note6: These pins of the module are not used and are internally suspended for processing.

Note7: The ModSelL is an input signal that shall be pulled to Vcc in the module. When held low by the host, the module responds to TWI serial communication commands. The ModSelL allows the use of multiple modules on a single TWI interface bus. When ModSelL is "High", the module shall not respond to or acknowledge any TWI interface communication from the host.

Note8: The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

Note9: TxDis signal requires to pull up 10k to Vcc inside the t module, indicating that the pump is turned off.

Note10: ModPrsL shall be pulled up to Vcc on the host board and pulled down to the GND in the module. The ModPrsL is asserted "Low" when the module is inserted. The ModPrsL is deasserted "High" when the module is physically absent from the host connector due to the pull-up resistor on the host board.

Note11: IntL is a open-collector output signal from the module. It shall be pulled-up 10k to Vcc on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read.